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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Rosengaus et al.

Attorney Docket No.: KLA1P001C1

Patent: 6,791,680 B1

Issued: September 14, 2004

Title: SYSTEM AND METHOD FOR INSPECTING SEMICONDUCTOR WAFERS

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on October 20, 2004 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____
Aurelia M. Sanchez

REQUEST FOR CERTIFICATE OF CORRECTION OF OFFICE MISTAKE (35 U.S.C. §254, 37 CFR §1.322)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Attn: Certificate of Correction

Dear Sir:

Attached is Form PTO-1050 (Certificate of Correction) at least one copy of which is suitable for printing. The errors together with the exact page and line number where they occur, and shown correctly in the application filed, are as follows:

SPECIFICATION:

1. Column 11, line 9, change "Fourier patte" to --Fourier pattern--. This appears correctly in the patent application as filed on page 15, line 10.

2. Column 11, line 23, change "criteria in bind" to --criteria in mind--. This appears correctly in the patent application as filed on page 15, line 19.

CLAIMS:

1. In line 4 of claim 9 (column 18, line 47) change "critical dimension" to --critical dimensions--. This appears correctly in Amendment H as filed on page 5, paragraph 5,line 3, old claim 77.

2. In line 10 of claim 12 (column 19, line 29) change "of inspection" to --of interleaved inspection--. This appears correctly in Amendment H as filed on page 4, paragraph 4, line 8.

Patentee hereby requests expedited issuance of the Certificate of Correction because the error lies with the Office and because the error is clearly disclosed in the records of the Office. As required for expedited issuance, enclosed is documentation that unequivocally supports the patentee's assertion without needing reference to the patent file wrapper.

It is noted that the above-identified errors were printing errors that apparently occurred during the printing process. Accordingly, it is believed that no fees are due in connection with the filing of this Request for Certificate of Correction. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. KLA1P001C1).

Respectfully submitted,
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NOV 2004

The spacing between individual vertical strips 706 may follow various mathematical progressions. For example, the spacing may vary logarithmically. In one specific embodiment, the spacing of the wires 706 in continuously variable filter tape 703 starts with a spacing of about 1 mm distance between the first wire (n=1) and the second (n=2). The space to the next wire (n+1) may be determined by the following equation:

$$\text{Distance}_{n=1} = \text{Distance}_n * (1 + Q) \qquad (2)$$

where Q is about 0.015 in a preferred embodiment. The maximum spacing of the pattern is determined by the aperture size of the Fourier plane such that a single wire could block a Fourier pattern containing a single spot. The total length of the tape is reasonable with about 15 inches being used for the preferred embodiment.

Generally, the spacing of Fourier transform spots in the Fourier plane is essentially equal across the plane. As indicated by equation 2, the wires in the filter increase slightly in spacing across the Fourier plane. Thus, the widths of the wires must be somewhat greater than the spot size at the image plane to account for both the accuracy to which the pattern can be positioned and the spacing difference between the wires across the Fourier plane. In practice, the Fourier image spots are often less than about 0.1 mm in diameter. Further, the positioning accuracy of a Fourier filter can be expected be less than about 0.05 mm. With these criteria in mind, the wire widths in filter tape 703 are preferably between about 0.2 and 0.6 mm. For example, a 0.35 mm wire width leaves about 0.2 mm available for the spacing difference across the aperture. Of course, other configurations having different width wires, spacings or separations, starting spacings, and change in spacings along the tape will have an equivalent effect.

Beyond the filter tape spacings indicated in Figures 7A and 7B, more complex patterns are possible (i.e. double periodicity, matched filtering, etc.). For example, Figure 7C presents double frequency Fourier filter tape 705 for use with this invention. In this case, two groups of vertical opaque strips are provided, each having a distinct spacing frequency. The first frequency is defined by regular spacing between vertical strips 710 and the second frequency is defined by vertical strips 712. Note that the spacing between vertical strips 712 is greater than the spacing between vertical strips 710.

A multiple frequency Fourier filter such as Fourier filter tape 705 is appropriate in the case where the region of the semiconductor wafer being imaged contains two or more overlaid repeating structures. This may be the case when, for

performing a second scan of the semiconductor wafer with the modular inspection tool wherein the metrology sensors are used to measure critical dimensions on the wafer.

74. (Previously Presented): A method of inspecting semiconductor wafers on a wafer handling chamber as recited in claim 73, further comprising:

transferring the semiconductor wafer from one of the plurality of wafer processing tools to the modular inspection tool.

75. (Previously Presented): A semiconductor manufacturing system as recited in claim 59, wherein the plurality of modular inspection subsystems are placed adjacent to one another such that each adjacent subsystem reviews a corresponding portion of the semiconductor wafer for defects.

76. (Previously Presented): A semiconductor manufacturing system as recited in claim 75, wherein at least two of the plurality of modular inspection subsystems perform the detection for defects simultaneously.

77. (Previously Presented): A semiconductor manufacturing system as recited in claim 59, wherein the measured parameters are selected from the group comprising of hot spots, deposition thicknesses, and critical dimensions.

78-80. (Canceled)

81. (Previously Presented): A semiconductor manufacturing system as recited in claim 73, wherein the plurality of interleaved inspection and metrology sensors are placed adjacent to one another such that each adjacent sensor reviews a corresponding portion of the semiconductor wafer.

82. (Previously Presented): A semiconductor manufacturing system as recited in claim 81, wherein at least two of the plurality of interleaved inspection and metrology sensors perform simultaneously.

83-84. (Canceled)

measuring the dimension of at least one feature on the semiconductor wafer with the metrology tool.

66. (Canceled)

67. (Previously Presented): A method of manufacturing a semiconductor wafer as recited in claim 65 wherein the metrology tool is an optical detector.

68. (Previously Presented): A semiconductor manufacturing system as recited in claim ~~59~~62 wherein the first metrology tool is an optical detector.

69-71. (Canceled)

72. (Currently Amended): A semiconductor manufacturing system**, comprising:** ~~as recited in 71~~

a wafer handling chamber having a plurality of facets, the wafer handling chamber containing a vacuum environment;

a plurality of wafer processing tools, each of the wafer processing tools being attached to a respective facet on the wafer handling chamber; and

a modular inspection tool attached to one of the facets of the wafer handling chamber, the modular inspection tool including a plurality of ~~wherein the inspection sensors and metrology sensors are~~ interleaved **inspection sensors and metrology sensors, whereby the metrology sensors measure critical dimensions on pattern-etched semiconductor wafers**.

73. (Previously Presented): A method of inspecting semiconductor wafers on a wafer handling chamber, comprising:

providing a wafer handling chamber having a plurality of facets, the wafer handling chamber containing a vacuum environment;

providing a plurality of wafer processing tools, each of the wafer processing tools being attached to a respective facet on the wafer handling chamber;

providing a modular inspection tool for attaching to a facet of the wafer handling chamber wherein the modular inspection tool includes a plurality of interleaved inspection and metrology sensors;

performing a first scan of a semiconductor wafer with the modular inspection tool wherein the inspection sensors are used to inspect the wafer for defects; and

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(Also Form PT-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,791,680 B1

DATED : September 14, 2004

INVENTOR(S) : Rosengaus et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the Specifications:

Column 11, line 9, change "Fourier patte" to --Fourier pattern--.
Column 11, line 23, change "criteria in bind" to --criteria in mind--.

In the Claims:

In line 4 of claim 9 (column 18, line 47) change "critical dimension" to --critical dimensions--.

In line 10 of claim 12 (column 19, line 29) change "of inspection" to --of interleaved inspection--.

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